

In the Claims:

Claims 1-11 (Canceled).

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Claim 12 (Previously Amended). The current source circuit according to claim 13, wherein said first driver stage forms a part of a current mirror circuit receiving a flow of a stabilized current when said first driver stage is switched on.

Claim 13 (Currently Amended). A controllable current source circuit, comprising:

an output;

a supply voltage terminal and a reference potential terminal;

a connection node;

a first driver stage having a first controlled path containing a first transistor and a second driver stage having a second controlled path containing a second transistor having a control terminal, said first and second controlled paths connected in series between said voltage supply terminal and said reference potential terminal, and said second driver stage forming a part of a first current mirror circuit causing a constant stabilized current to flow in said second driver

stage[; and], only said first driver stage switching on and off in dependence on an input signal, and said second driver stage being switched on and carrying a stabilized current;

at least two current paths connected between said connection node and said reference potential terminal, each of said at least two current paths including a further transistor having a respective control terminal, said control terminals of said further transistors being connected to said control terminal of said second transistor;

a phase comparator stage being connected between said connection node and said voltage supply terminal and including a switching element and at least two current paths connecting said switching element to said voltage supply terminal; and

a second current mirror circuit having a primary side and a secondary side;

one of said current paths of said phase comparator stage including said primary side of said second current mirror circuit; and

said secondary side of said second current mirror circuit including said first transistor.

Claim 14 (Previously Amended). The current source circuit according to claim 13, wherein said current mirror circuit is coupled to a current mirror circuit connected to said first driver stage and causes a current to flow in said current mirror circuit connected to said first driver stage.

Claim 15 (Previously Added). The current source circuit according to claim 13, wherein a current carried by said first driver stage when said first driver stage is switched on is greater than a current carried by said second driver stage.

Claim 16 (Previously Added). The current source circuit according to claim 15, wherein the current carried in said first driver stage is multiple times greater than the current carried by said second driver stage.

Claim 17 (Previously Added). The current source circuit according to claim 15, wherein the current carried in said first driver stage is four times greater than the current carried by said second driver stage.

Claim 18 (Previously Amended). A phase locked loop, comprising:

a phase comparator having a phase comparison circuit with a reference signal input for receiving a reference signal and an

input for receiving an input signal whose phase angle is to be regulated, and having a controllable current source circuit according to claim 13 on an output side of said phase comparator;

a loop filter connected to said current source circuit and having an output for outputting an output signal controlling the phase angle of the input signal.

Claim 19 (Previously Added). The phase locked loop according to claim 18, wherein said phase comparison circuit contains a comparator configured to switch between two output states and having a single output terminal connected to said current source circuit.

Claim 20 (Previously Added). The phase locked loop according to claim 18, wherein said phase comparison circuit contains an exclusive-OR gate.

Claim 21 (Previously Added). The phase locked loop according to claim 18, which comprises a current mirror circuit connected to said phase comparison circuit for stabilizing a current flowing into said phase comparison circuit and into said second driver stage.

Claim 22 (Previously Added). The phase locked loop according to claim 18, wherein said first driver stage of said controllable current source circuit forms a part of a current mirror circuit receiving a flow of a stabilized current when said first driver stage is switched on.

Claim 23 (Previously Added). The phase locked loop according to claim 18, wherein said current mirror circuit of said controllable current source circuit is coupled to a current mirror circuit connected to said first driver stage and causes a stabilized current to flow in said current mirror circuit connected to said first driver stage.

Claim 24 (Previously Added). The phase locked loop according to claim 18, wherein a current carried by said first driver stage of said controllable current source circuit when said first driver stage is switched on is greater than a current carried by said second driver stage.

Claim 25 (Previously Added). The phase locked loop according to claim 24, wherein the current carried in said first driver stage of said controllable current source circuit is multiple times greater than the current carried by said second driver stage.

Claim 26 (Previously Added). The phase locked loop according to claim 24, wherein the current carried in said first driver stage of said controllable current source circuit is four times greater than the current carried by said second driver stage.

Claim 27 (Previously Added). The current source circuit according to claim 14, wherein said second driver stage includes:

a circuit node;

a control electrode;

a first and a second current path connected between said supply voltage terminal and said circuit node;

one of said first and said second current paths forming a part of said current mirror circuit connected to said first driver stage; and

a transistor connected between said circuit node and said reference potential terminal, said transistor having a transistor control electrode connected to said control electrode of said second driver stage.